UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/966,889	09/28/2001	Robert A. Lester	COMP:0234 P01-3624	4331

7590 09/29/2004

Intellectual Property Administration
Legal Department, M/S 35
PO Box 272400
Ft. Collins, CO 80527-2400

EXAMINER	
CLEARY, THOMAS J	

ART UNIT	PAPER NUMBER
2111	

DATE MAILED: 09/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/966,889	LESTER ET AL.	
	Examiner	Art Unit	
	Thomas J. Cleary	2111	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 29 June 2004.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-19 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-19 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on 28 September 2001 is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1, 6, 12, and 16 are rejected under 35 U.S.C. 103(a) as being unpatentable over US Patent Number 5,802,269 to Poisner et al. ("Poisner") and US Patent Number 6,272,601 to Nunez et al. ("Nunez").

3. In reference to Claim 1, Poisner teaches a system comprising: a processor (See Figure 2 Number 31); a main memory operably coupled to the processor (See Figure 2 Number 35); a cache memory operably coupled to the processor (See Figure 2 Number 39); and a bridge, which is equivalent to a host controller, coupled between the processor and the main memory (See Figure 2 Number 33); the host controller comprising: a memory controller operably coupled to the main memory (See Column 3 Lines 61-63); a processor controller operably coupled to the processor (See Column 3 Lines 64-67); and a coherency controller operably coupled to the cache memory (See Column 3 Lines 61-63). Poisner further teaches that the bridge facilitates

communications between the processor, the main memory, and the cache memory (See Column 3 Lines 59-67), and thus it inherently includes an internal bus structure configured to couple each of the memory controller, the processor controller, and the coherency controller to each other. Poisner does not teach wherein each of the individual buses comprises a unidirectional bus configured to transmit only one signal type. Nunez teaches the use of an interconnect comprised of buses that are unidirectional and that carry only one type of signal, namely, address or data (See Column 8 Lines 1-2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner with the unidirectional interconnect buses of Nunez, resulting in the invention of Claim 1, in order to improve performance by eliminating the need for buffers and tri-state drivers typically associated with bi-directional buses (See Column 8 Lines 1-4 of Nunez).

4. In reference to Claim 6, Poisner and Nunez teach the limitations as in Claim 1 above. Nunez further teaches that each of the plurality of individual buses is configured to transmit only one respective signal type, namely a data signal type or an address signal type (See Column 8 Lines 1-4). Further, the data signals and address signals of Nunez inherently correspond to a single transaction in an operation.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner with the unidirectional interconnect buses of Nunez, resulting in the invention of Claim 6, in order to improve

performance by eliminating the need for buffers and tri-state drivers typically associated with bi-directional buses (See Column 8 Lines 1-4 of Nunez).

5. In reference to Claim 12, Poisner teaches a bridge containing first and second controllers that communicate with each other and thus inherently has an internal bus structure comprising a plurality of individual buses (See Column 3 Lines 59-67). Poisner does not teach that the individual buses comprise a unidirectional bus configured to transmit only one signal type. Nunez teaches the use of an interconnect comprised of buses that are unidirectional and that carry only one type of signal, namely, address or data (See Column 8 Lines 1-2).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner with the unidirectional interconnect buses of Nunez, resulting in the invention of Claim 12, in order to improve performance by eliminating the need for buffers and tri-state drivers typically associated with bi-directional buses (See Column 8 Lines 1-4 of Nunez).

6. In reference to Claim 16, Poisner and Nunez teach the limitations as in Claim 12 above. Nunez further teaches that each of the individual buses is configured to transmit only one respective signal type, namely a data signal type or an address signal type (See Column 8 Lines 1-4). Further, the data signals and address signals of Nunez inherently correspond to a single transaction in an operation.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner with the unidirectional interconnect buses of Nunez, resulting in the invention of Claim 16, in order to improve performance by eliminating the need for buffers and tri-state drivers typically associated with bi-directional buses (See Column 8 Lines 1-4 of Nunez).

7. Claims 2, 3, 4, 5, 13, 14, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner and Nunez as applied to Claims 1 and 12 above, and further in view of US Patent Application Publication Number 2002/0073261 to Kosaraju ("Kosaraju").

8. In reference to Claim 2, Poisner and Nunez teach the limitations as applied to Claim 1 above. Poisner and Nunez do not teach that the plurality of individual busses is coupled only between two of the memory controller, the processor controller, and the coherency controller. Kosaraju teaches connecting devices together using a point-to-point bus in which each device is connected to only one other device (See Page 2 Paragraph 24).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Poisner and Nunez using the point-to-point bus architecture of Kosaraju, resulting in the invention of Claim 2, in order to provide an uninterrupted connection between the two devices and provide a higher bandwidth connection between the two devices (See Page 1 Paragraph 3 of Kosaraju).

9. In reference to Claim 3, Poisner, Nunez, and Kosaraju teach the limitations as in Claim 2 above. Poisner further teaches that the bridge facilitates communications between the processor and the main memory, (See Column 3 Lines 59-67), and thus it inherently includes the plurality of individual buses coupled between the memory controller and the processor controller.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Poisner and Nunez using the point-to-point bus architecture of Kosaraju, resulting in the invention of Claim 3, in order to provide an uninterrupted connection between the two devices and provide a higher bandwidth connection between the two devices (See Page 1 Paragraph 3 of Kosaraju).

10. In reference to Claim 4, Poisner, Nunez, and Kosaraju teach the limitations as in Claim 2 above. Poisner further teaches that the bridge facilitates communications between the cache memory and the main memory, (See Column 3 Lines 59-67), and thus it inherently includes the plurality of individual buses coupled between the memory controller and the coherency controller.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Poisner and Nunez using the point-to-point bus architecture of Kosaraju, resulting in the invention of Claim 4, in order to provide an uninterrupted connection between the two devices and provide a higher bandwidth connection between the two devices (See Page 1 Paragraph 3 of Kosaraju).

11. In reference to Claim 5, Poisner, Nunez, and Kosaraju teach the limitations as in Claim 2 above. Poisner further teaches that the bridge facilitates communications between the processor and the cache memory, (See Column 3 Lines 59-67), and thus it inherently includes the plurality of individual buses coupled between the processor controller and the coherency controller.

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Poisner and Nunez using the point-to-point bus architecture of Kosaraju, resulting in the invention of Claim 2, in order to provide an uninterrupted connection between the two devices and provide a higher bandwidth connection between the two devices (See Page 1 Paragraph 3 of Kosaraju).

12. In reference to Claim 13, Poisner and Nunez teach the limitations as applied to Claim 12 above. Poisner and Nunez do not teach that each individual bus is coupled between only a first controller and a second controller. Kosaraju teaches connecting devices together using a point-to-point bus in which each device is connected to only one other device (See Page 2 Paragraph 24).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Poisner and Nunez using the point-to-point bus architecture of Kosaraju, resulting in the invention of Claim 13, in order to provide an uninterrupted connection between the two devices and provide a higher bandwidth connection between the two devices (See Page 1 Paragraph 3 of Kosaraju).

13. In reference to Claim 14, Poisner, Nunez, and Kosaraju teach the limitations as applied to Claim 13 above. Poisner further teaches that the first controller comprises a processor controller (See Column 3 Lines 64-67).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Poisner and Nunez using the point-to-point bus architecture of Kosaraju, resulting in the invention of Claim 14, in order to provide an uninterrupted connection between the two devices and provide a higher bandwidth connection between the two devices (See Page 1 Paragraph 3 of Kosaraju).

14. In reference to Claim 15, Poisner, Nunez, and Kosaraju teach the limitations as applied to Claim 13 above. Poisner further teaches that the second controller comprises a memory controller (See Column 3 Lines 61-63).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Poisner and Nunez using the point-to-point bus architecture of Kosaraju, resulting in the invention of Claim 15, in order to provide an uninterrupted connection between the two devices and provide a higher bandwidth connection between the two devices (See Page 1 Paragraph 3 of Kosaraju).

15. Claims 7, 8, 17, and 18 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner and Nunez as applied to Claims 6 and 16 above, and further in view of US Patent Number 6,584, 031 to Hanaoka et al. ("Hanaoka").

16. In reference to Claim 7, Poisner and Nunez teach the limitations as applied to Claim 6 above. Poisner and Nunez do not teach that each respective signal type includes an identification tag. Hanaoka teaches the use of a header that provides an identification tag for data communicated across a serial interface (See Figure 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner and Nunez with the header of Hanaoka, resulting in the invention of Claim 18, in order allow the data to be sent in a well-known packet format that can provide information to the receiver regarding the data as well as provide a cyclic redundancy check of the data to insure proper receipt (See Figure 4 of Hanaoka).

17. In reference to Claim 8, Poisner, Nunez, and Hanaoka teach the limitations as applied to Claim 7 above. Hanaoka further teaches that the identification tag comprises a source identification, a destination identification, and a priority identification, which is equivalent to a cycle identification (See Figure 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner and Nunez with the header of Hanaoka, resulting in the invention of Claim 18, in order allow the data to be sent in a well-known packet format that can provide information to the receiver regarding the data as well as provide a cyclic redundancy check of the data to insure proper receipt (See Figure 4 of Hanaoka).

18. In reference to Claim 17, Poisner and Nunez teach the limitations as applied to Claim 16 above. Poisner and Nunez do not teach that each signal type includes an identification tag. Hanaoka teaches the use of a header that provides an identification tag for data communicated across a serial interface (See Figure 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner and Nunez with the header of Hanaoka, resulting in the invention of Claim 18, in order allow the data to be sent in a well-known packet format that can provide information to the receiver regarding the data as well as provide a cyclic redundancy check of the data to insure proper receipt (See Figure 4 of Hanaoka).

19. In reference to Claim 18, Poisner, Nunez, and Hanaoka teach the limitations as applied to Claim 17 above. Hanaoka further teaches that the identification tag comprises a source identification, a destination identification, and a priority identification, which is equivalent to a cycle identification (See Figure 4).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner and Nunez with the header of Hanaoka, resulting in the invention of Claim 18, in order allow the data to be sent in a well-known packet format that can provide information to the receiver regarding the data as well as provide a cyclic redundancy check of the data to insure proper receipt (See Figure 4 of Hanaoka).

20. Claims 9 and 19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner, Nunez, and Hanaoka as applied to Claims 8 and 18 above, and further in view of US Patent Number 6,130,886 to Ketseoglou et al. ("Ketseoglou").

21. In reference to Claim 9, Poisner, Nunez, and Hanaoka teach the limitations as applied to Claim 8 above. Poisner, Nunez, and Hanaoka do not teach that the cycle identification comprises a toggle bit configured to free the cycle identification for re-use before each transaction in the request operation is complete. Ketseoglou teaches a correlative ID field that appears in signal messages until the link is dropped and can be changed during a connection, and thus enables reuse of the identification before the operation is complete (See Column 11 Lines 60-62 and Column 13 Lines 57-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner, Nunez, and Hanaoka with the reusable identification numbers of Ketseoglou, resulting in the invention of Claim 9, in order to allow reuse of the number before the connection is completed (See Column 13 Lines 56-61 of Ketseoglou).

22. In reference to Claim 19, Poisner, Nunez, and Hanaoka teach the limitations as applied to Claim 18 above. Poisner, Nunez, and Hanaoka do not teach that the cycle identification comprises a toggle bit configured to free the cycle identification for re-use before each transaction in the request operation is complete. Ketseoglou teaches a

correlative ID field that appears in signal messages until the link is dropped and can be changed during a connection, and thus enables reuse of the identification before the operation is complete (See Column 11 Lines 60-62 and Column 13 Lines 57-61).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner, Nunez, and Hanaoka with the reusable identification numbers of Ketseoglou, resulting in the invention of Claim 19, in order to allow reuse of the number before the connection is completed (See Column 13 Lines 56-61 of Ketseoglou).

23. Claim 10 is rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner and Nunez as applied to Claim 1 above, and further in view of US Patent Number 5,901,281 to Miyao et al. ("Miyao").

24. In reference to Claim 10, Poisner and Nunez teach the limitations as applied to Claim 1 above. Poisner and Nunez do not teach that the processor comprises the cache memory. Miyao teaches using a processor that has an internal cache (See Column 3 Lines 24-27).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to construct the device of Poisner and Nunez with the processor internal cache of Miyao, resulting in the invention of Claim 10, because recent microprocessors generally contain internal cache memories because of improved integration (See Column 3 Lines 24-27 of Miyao).

25. Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Poisner and Nunez as applied to Claim 1 above, and further in view of US Patent Number 6,587,930 to Deshpande et al. ("Deshpande").

26. In reference to Claim 11, Poisner and Nunez teach the limitations as applied to Claim 1 above. Poisner and Nunez do not teach a plurality of processor buses; a plurality of processing units, wherein each processing unit is coupled to a respective one of the plurality of processor buses; and a plurality of processor controllers, each processor controller corresponding to a respective one of the plurality of processor buses, wherein the processor controllers are not directly coupled to each other via the internal bus structure. Deshpande teaches a plurality of processor buses (See Figure 4 Numbers 413 and 414); a plurality of processing units, wherein each processing unit is coupled to a respective one of the plurality of processor buses (See Figure 4 Numbers 411 and 412); a plurality of processor controllers, each processor controller corresponding to a respective one of the plurality of processor buses (See Figure 6), and wherein the processor controllers are not directly coupled to each other via the internal bus structure (See Figure 6).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the device of Poisner and Nunez with the plurality of processing units, processing buses, and processing controllers of Deshpande, resulting in the invention of Claim 11, in order to increase the speed and reliability of the system

by utilizing multiple processors as well as to help maintain cache coherency by preventing read-read deadlocks (See Abstract of Deshpande).

Response to Arguments

27. Applicant's arguments filed 29 June 2004 have been fully considered but they are not persuasive.

28. In reference to the Applicant's arguments with regards to Claims 1, 6, 12, and 16 that the Poisner reference does not inherently disclose "an internal bus structure configured to couple each of the memory controller, the processor controller, and the coherency controller to each other" (See Pages 7-11), the Examiner notes that the bridge disclosed by Poisner (Figure 2 Number 33) is a host bridge, or North bridge, circuit coupled between the host bus an a PCI bus. The use of such a bridge is supported in the specification as being well known in the art, as it conforms to the Peripheral Component Interconnect architecture, such as Revision 2.1 promulgated by Intel Corporation, 1995. It is further well known that a bridge conforming to said PCI architecture will have an internal bus structure allowing signals to be communicated between the external busses, such as the host bus, cache bus, and main memory bus used by Poisner. The Applicant has not provided evidence that a bridge such as the one used by Poisner would not inherently include an internal bus structure, and thus, the traversal of the rejections is not considered persuasive.

29. In reference to the Applicant's arguments with respect to Claims 1, 6, 12, and 16 that the Nunez reference does not disclose "a host controller having a memory controller, a process controller, a coherency controller, or any internal bus structure for coupling such controllers" (See Pages 11-12), the Examiner notes that Poisner, and not Nunez, is being relied upon to disclose these limitations.

30. In reference to the Applicant's arguments with respect to Claims 1, 6, 12, and 16 that the Nunez reference does not teach "an internal bus structure comprising individual buses each having a unidirectional bus configured to transmit only one signal type" (See Pages 12-13), the Examiner notes that the Applicant has admitted that Nunez discloses unidirectional address and data buses. The address signal on the address bus is one type of signal, and the data signal on the data bus another type of signal. As such, the address bus is only configured to transmit signals of the address signal type, and the data bus is only configured to transmit signals of the data signal type. As the address bus is separate from the data bus, each bus constitutes an individual bus. The Examiner further notes that the features upon which Applicant relies (i.e., the internal bus structure provides point-to-point connections of the individual buses, each carrying a unique signal associated with a particular transaction; and the signal types including a request address/command signal, an initial response signal, a request snoop results signal, a snoop address signal, etc.) are not recited in the rejected claim(s). Although the claims are interpreted in light of the specification, limitations from the specification

are not read into the claims. See *In re Van Geuns*, 988 F.2d 1181, 26 USPQ2d 1057 (Fed. Cir. 1993).

31. In reference to the Applicant's arguments with respect to Claims 2-5 and 13-15 that the Kosaraju reference does not teach "connecting devices together using a point-to-point bus, wherein each device is connected to only one other device" (See Pages 13-14), the Examiner notes that Kosaraju teaches that each bus is a point-to-point bus which is coupled only between two devices (See Figures 3-5, and Page 2 Paragraphs 19 and 22-24). The Examiner further notes that the combination of Poisner and Nunez, and not Kosaraju, is being relied upon to disclose the specific connectivity between the memory controller, processor controller, and coherency controller as claimed. Kosaraju is being relied upon to disclose that the use of a point-to-point bus architecture is well known, and as shown above, it would be obvious to one of ordinary skill in the art to use a point-to-point bus with the device created by the combination of Poisner and Nunez.

32. In reference to the Applicant's arguments with respect to Claims 7, 8, 17, and 18 that the Hanaoka reference does not disclose "the internal bus structure comprising a plurality of individual buses, and wherein each of the individual buses comprises a unidirectional bus configured to transmit only one signal type" (See Pages 14-15), the Examiner notes that Poisner and Nunez, and not Hanaoka, are being relied upon to disclose these limitations.

33. In reference to Applicant's arguments with respect to Claims 9 and 19 that the Ketseoglou reference does not teach "that the cycle identification comprises a toggle bit configured to free the cycle identification for re-use before each transaction in the request operation is complete" (See Pages 15-16), the Examiner notes that Ketseoglou teaches a correlative ID, which is equivalent to a cycle identification, that indicates that it can be released for re-use at the termination of a connection or that it can be changed during the connection, thus freeing the correlative ID that was changed for re-use (See Column 13 Lines 55-63).

34. In reference to the Applicant's arguments with respect to Claim 10 that the Miyao reference does not disclose "the processor controller, the internal bus structure comprising a plurality of individual buses, and wherein each of the individual buses comprises a unidirectional bus configured to transmit only one signal type" (See Page 17), the Examiner notes that Poisner and Nunez, and not Miyao, are being relied upon to disclose these limitations.

35. In reference to the Applicant's arguments with respect to Claim 11 that the Deshpande reference does not disclose "the processor controller, the internal bus structure comprising a plurality of individual buses, and wherein each of the individual buses comprises a unidirectional bus configured to transmit only one signal type" (See Pages 17-18), the Examiner notes that Poisner and Nunez, and not Deshpande, are being relied upon to disclose these limitations.

Drawings

36. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, a.) wherein each respective signal type includes an identification tag, as in Claims 7 and 17; b.) wherein the identification tag comprises a source identification, a destination identification, and a cycle identification, as in Claims 8 and 18; c.) wherein the cycle identification comprises a toggle bit configured to free the cycle identification for re-use before each transaction in the request operation is complete, as in Claims 9 and 19; and d.) wherein the processor comprises the cache memory, as in Claim 10, must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement

Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the Examiner, the Applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Conclusion

37. **THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the Examiner should be directed to Thomas J. Cleary whose telephone number is 703-305-5824. The Examiner can normally be reached on Monday-Thursday (7-4), Alt. Fridays (7-3).

If attempts to reach the Examiner by telephone are unsuccessful, the Examiner's supervisor, Mark H. Rinehart can be reached on 703-305-4815. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306. Beginning November 2004, the Examiner's telephone number will be changing to 571-272-3624, and the Examiner's supervisor's telephone number will be changing to 571-272-3632.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

TJC

MARK H. RINEHART
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100

Thomas J. Cleary
Patent Examiner
Art Unit 2111